

US-PAT-NO: 6525609
DOCUMENT-IDENTIFIER: US 6525609 B1
TITLE: Large gain range, high linearity, low noise MOS VGA

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Brief Summary Text - BSIX (2):

Radio receivers, or tuners, are widely used in applications requiring the reception of electromagnetic energy. Applications can include broadcast receivers such as radio and television, set top boxes for cable television, receivers in local area networks, LANs, and measurement equipment, radar receivers, air traffic control receivers, and microwave communication links among others. Transmission of the electromagnetic energy may be over a transmission line or by electromagnetic radio waves.

Drawing Description Text - DRIX (60):

FIGS. 49a and 49b are illustrations of an embodiment of compensation circuitry used to activate individual LNA amplifier stages:

Detailed Description Text - DETX (13):

This type of resonant circuit used as a preselector will increase frequency selectivity of a receiver that has been designed with this stage at its input. If an active preselector circuit is used between an antenna and frequency conversion stages, the sensitivity of the receiver will be increased as well as improving selectivity. If a signal is weak its level will be close to a background noise level that is present on an antenna in addition to a signal.

If this signal cannot be separated from the noise, the radio signal will not be able to be converted to a signal usable by the receiver. Within the receiver's signal processing chain, the signal's amplitude is decreased by losses at every stage of the processing. To make up for this loss the signal can be amplified initially before it is processed. Thus, it can be seen why it is desirable to provide a circuit in the receiver that provides frequency selectivity and

provide a circuit in the receiver that provides frequency selectivity and

Document ID	Kind Codes	Source	Issue Date	Pages	Links
US 6525609 B1		USPAT	20030121	123	Links
US 6509798 B2		USPAT	20030121	179	Varia
US 6500715 B2		USPAT	20021231	C2	Metho
US 6466634 B1		USPAT	20021015	58	Radio
US 6445039 B1		USPAT	20020903	100	Syste
US 6426630 B1		USPAT	20020730	151	Syste
US 6394649 B1		USPAT	20020517	3333	Radio
US 6351193 B1		USPAT	20020226	3343	Stran

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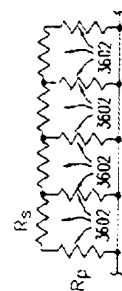


FIG. 39

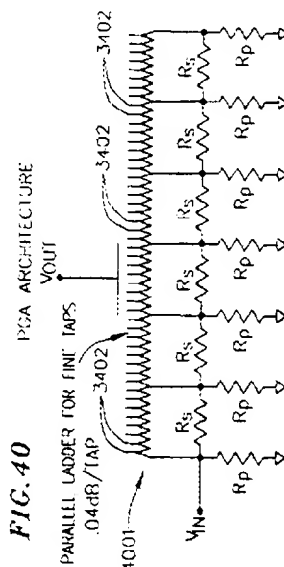


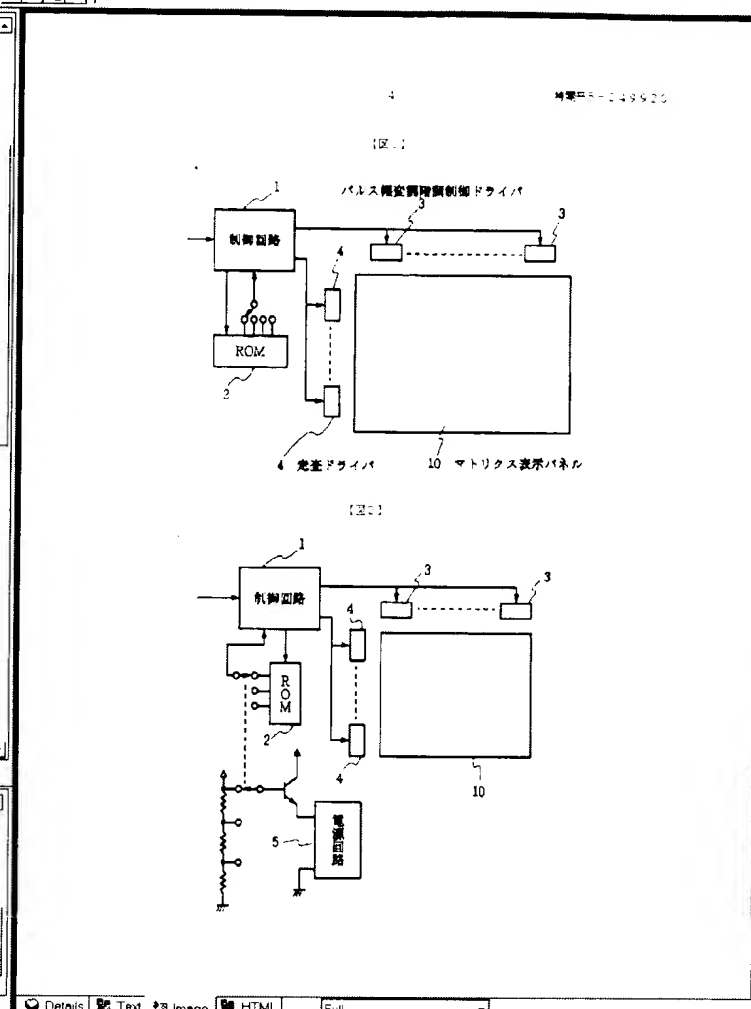
FIG. 40

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CONSTITUTION: A gradation control driver 3 by means of pulse width modulation and a scanning driver 4 are connected to a matrix display panel 10 composed of plural number of electrodes. A control circuit 1 addresses to a ROM 2, and reads gradation clocks in a single horizontal period, and transmits them to the gradation driver 3. At this time, which clocks the ROM 2 are adapted is determined according to respective display devices. The control circuit 1 counts the number of clocks corresponding to display data of respective picture elements, and determines a corresponding pulse width, and addresses pulses on the picture elements, and control is carried out by changing the magnitude of effective voltage applied to the picture elements. In this case, to put it concretely, the ROM 2 writes clock data in the ROM having a bit length of four bits, and selection of bits is carried out by means of upper wires.

Document Identifier - DID (1):

Current US Cross Reference Classification - CCXR (1):



Details		Text	Image	HTML	FWAC	
	U	1	Document ID	Issue Dat	Pages	Tit
3	<input type="checkbox"/>	<input type="checkbox"/>	JP 02353170	19901011	1	LIQUID CRYSTAL DRIVER CHE
	<input type="checkbox"/>	<input type="checkbox"/>	JP 05249920	19930913	6	DRIVING CIRCUIT FOR LIQUI
10	<input type="checkbox"/>	<input type="checkbox"/>	JP 05173503	19930713	10	DATA DRIVER CIRCUIT FOR L
11	<input type="checkbox"/>	<input type="checkbox"/>	JP 04102892	19930403	11	DRIVING CONTROL SYSTEM FO
	<input type="checkbox"/>	<input type="checkbox"/>	A			DEVICE
Details		Text	Image	HTML		

DATA 11.54 CIRCUIT FOR 11.54 * 11.54 DISPLAY DEVICE

	U	1	Document ID	Issue Dat	Pages	Ti
7	U	A	US 5892494	19900405	19	Correction of LCD drive v
8	U	A	JP 02053170	19901011	1	LCD switching element tur LIQUID CRYSTAL DRIVER CIR
9	U	A	JP 05149920	19930928	6	DRIVING CIRCUIT FOR LIQU
10	U	A	JP 05173503	19930713	11	DATA DRIVER CIRCUIT FOR L
11	U	A	JP 01133554	19930402	11	DEVICE

PAT NO: JP405173503A

DOCUMENT-IDENTIFIER: JP 05173503 A

TITLE: DATA DRIVER CIRCUIT FOR LIQUID CRYSTAL DISPLAY DEVICE

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Abstract Text - FPAR (2):

CONSTITUTION: In the data driver circuit 20 of a liquid crystal display device 25 provided with a first and a second latch 22, 23, having the capacity corresponding by one display row of the image data of an interface system and transferring the image data from the first latch 22 to the second latch 23 after fetching the image data by one display row into the first latch 22 and selecting a second reading data of one side of the output of the second latch 23 and applying it to a polarity inverting means 24, a circuit for replacing means 25 reading twice the holding content of the second latch 23 and providing a polarity inverting means 24 inverting the polarity of the reading data of one side and further replacing the order of the data of one side and further replacing the order of the data of one side corresponding to the reading data of one side is provided.

Details Text Image HTML KWIC

	U	1	Document ID	Issue Dat	Pages	Ti
6	<input type="checkbox"/>	<input checked="" type="checkbox"/>	JP 05249920	19930928	6	DRIVING CIRCUIT FOR LIQUID CRYSTAL DISPLAY DEVICE
7	<input type="checkbox"/>	<input checked="" type="checkbox"/>	JP 05224626	19930903	7	LIQUID CRYSTAL DISPLAY DEVICE
8	<input type="checkbox"/>	<input checked="" type="checkbox"/>	JP 05203918	19930813	5	ACTIVE MATRIX LIQUID CRYSTAL DISPLAY DEVICE
9	<input type="checkbox"/>	<input checked="" type="checkbox"/>	JP 05173503	19930713	12	DATA DRIVER CIRCUIT FOR LIQUID CRYSTAL DISPLAY DEVICE
10	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	JP 05119744	19930518		LIQUID CRYSTAL DISPLAY DEVICE

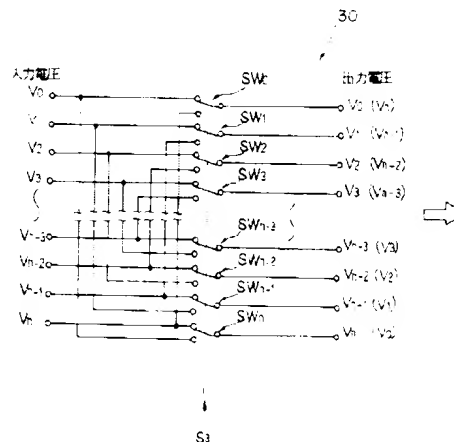
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申請番号 173503

(図1)

第2実施例の階調電圧反転回路の構成図



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Full

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Abstract Text - FPAR (2):

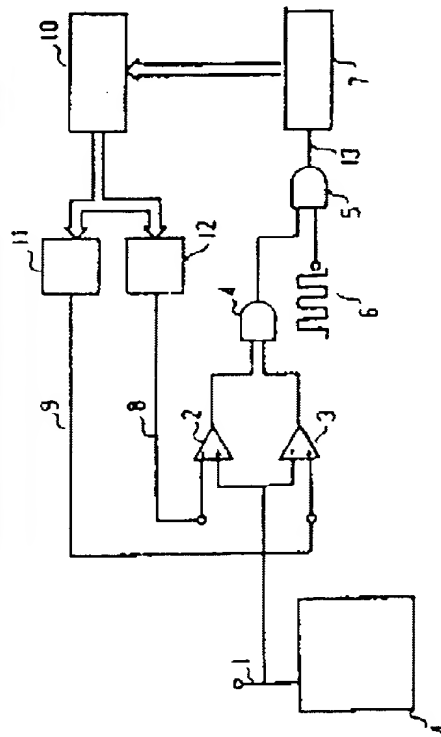
CONSTITUTION: First and second differential amplifiers 2 and 3 activate an AND gate 4 when an output signal 1 of the LCD driver is between an upper limit set voltage 8 and a lower limit set voltage 9 generated by D/A converters 11 and 12. An AND gate 5 acts to permit the input of a clock 6 to a clock counting circuit 7 only when the output of the gate 4 is in the active state. A GPU 10 reads the output value of the counting circuit 7 to detect the time of the signal of the LCD driver output stage outputted between the upper limit set voltage 8 and the lower limit set voltage 9. Thus, the output processing functions (the output value and the time of the occurrence of the output stage) of the LCD driver are simultaneously measured.

Title of Patent Publication - TTL (1):

LIQUID CRYSTAL DRIVER CHECKING CIRCUIT

Current US Cross Reference Classification - CCXR (1):

G06F1/00



Details Text Image HTML KWIC

Document ID	Kind Codes	Source	Issue Date	Pages
JP 02253170 A		JPO	19901011	1 LIQUID

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DOCUMENT-IDENTIFIER: US 20020126076 A1

TITLE: Liquid crystal display device and method of driving the same

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Claims Text - CLTM 100:

1. A liquid crystal display device comprising: (a) a first substrate; (b) a second substrate; (c) a liquid crystal layer sandwiched between said first and second substrates; (d) a plurality of scanning lines arranged on said first substrate; (e) a plurality of signal lines arranged on said first substrate; (f) a plurality of first switches arranged at intersections of said scanning lines and said signal lines; (g) a plurality of pixel electrodes each electrically connected to each of said first switches; (h) a plurality of driving electrodes each arranged in parallel with each of said pixel electrodes; and (i) a signal line driver which switches a first voltage for driving a positive pole and a second voltage for driving a negative pole at a predetermined interval in accordance with a first and second input, and outputs said positive or negative driving voltage to said signal lines, said signal line driver compensating for said first and second input.

Patent Application Publication Sep. 12, 2002 Sheet 15 of 30 US 2002/0126076 A1

FIG.18

GRADATION	REFERENCE	POSITIVE POLE	NEGATIVE POLE	AVERAGE	GRADATION COMPRESSION
255	REFERENCE 1	11.00V	0.60V	5.8V	-
254	REFERENCE 2	9.97V	1.63V	5.8V	-
240	REFERENCE 3	9.41V	2.19V	5.8V	-
192	REFERENCE 4	8.66V	2.94V	5.8V	-
128	REFERENCE 5	7.93V	3.67V	5.8V	-
84	REFERENCE 6	7.05V	4.55V	5.8V	-
32	REFERENCE 7	6.00V	5.30V	5.8V	-
0	REFERENCE 8	5.80V	5.80V	5.8V	-

	U	1	Document ID	Issue Dat	Pages	Tit
	<input type="checkbox"/>	<input type="checkbox"/>	US 20020126076	20020913	50	Liquid crystal display de the same
4	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 20020109656	20020819	10	Liquid crystal display de thereof
5	<input type="checkbox"/>	<input type="checkbox"/>	US 20020075273	20020820	22	Display control device and apparatus
6	<input type="checkbox"/>	<input type="checkbox"/>	US 20020050972	20020502	16	Dot-inversion data driver display device
7	<input type="checkbox"/>	<input type="checkbox"/>	US 20020050972	20020507	11	Shift register and drivin